CHIP TO CHIP INTERFACE FOR INTERCONNECTING CHIPS

ABSTRACT

A Network Processor (NP) is formed from a plurality of operatively coupled chips. The NP includes a Network Processor Complex (NPC) Chip coupled to a Data Flow Chip and Data Store Memory coupled to the Data Flow Chip. An optional Scheduler Chip is coupled to the Data Flow Chip. The named components are replicated to create a symmetric ingress and egress structure. Communications between the chips are provided by a pair of Chip to Chip Macros, one of each operatively positioned on one of the chips, and a Chip to Chip Bus Interface operatively coupling the Chip to Chip Macros.